AMENDMENTS TO THE CLAIMS

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1.-17. (canceled)

18. (previously presented) A data processing system comprising:

a system controller having:

a first memory channel controller;

a second memory channel controller; and

a high-speed bus arbiter;

an input output (IO) controller in communication with the high-speed bus arbiter via a high speed bus, and having a low-speed bus arbiter coupled to a low speed bus, wherein the low-speed bus arbiter supports a slower bus rate than the high-speed bus arbiter, and a separate bus that is not coupled to the low speed bus arbiter and coupled to a data storage device.

19. (previously presented) The system of claim 18, wherein a bus rate of the high-speed bus arbiter is at least 10 percent faster than the bus rate of the low-speed bus arbiter.

20. (previously presented) The system of claim 19, wherein the bus rate of the high-speed bus arbiter is approximately 66 Mbits per second per data pin and the bus rate of the low-speed bus arbiter is approximately 33 Mbits per second per data pin.

21. – 23. (canceled)

24. (previously presented) A data processing system comprising:

a system controller having:

a first memory channel controller;

a second memory channel controller;

a high-speed bus arbiter;

an input output (IO) controller in communication with the high-speed bus arbiter via a first high speed bus, and having a low-speed bus arbiter, wherein the low-speed arbiter supports a slower bus rate than the high-speed bus arbiter; and

a data storage device coupled to the I/O controller via a different bus to transmit data at a data rate higher than the data rate of the low-speed bus arbiter.

25. (previously presented) The data processing system of claim 18 wherein the system controller comprises a graphics engine and wherein the data processing system includes a unified memory coupled to the first memory channel controller and the second memory channel controller wherein the unified memory is controlled to store both graphics data and system data.